REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, Claims 1-30 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 5,856,229 to Sakaguchi, et al. ("Sakaguchi, et al.") and U.S. Patent No. 5,528,397 to Zavracky, et al. ("Zavracky, et al.").

Applicants respectfully submit that the methods recited in Claims 1-30 are not made obvious from the combined disclosures of Sakaguchi, et al. and Zavracky, et al. In particular, the combined disclosures of Sakaguchi, et al. and Zavracky, et al. do not teach or suggest the processing steps recited in Claims 1-13 of the present application. Specifically, Sakaguchi, et al. and Zavracky, et al. do not teach or suggest a method that includes the steps of selecting a first substrate including a base substrate and at least a partially crystalline porous release layer; forming a semiconductor layer on the porous release layer, said semiconductor layer having a bottom surface in contact with the porous release layer and an upper surface; forming at least one semiconductor device in the upper surface layer of the semiconductor layer; bonding the upper surface of the semiconductor layer to a temporary auxiliary substrate; detaching the semiconductor layer from said first substrate by breaking apart the porous layer; bonding the bottom surface of the semiconductor layer to a final substrate; and detaching the semiconductor layer from the temporary auxiliary substrate. Thus, in the processing steps recited in Claims 1-13 of the present application two separate bonding and detaching steps as well as three substrates, i.e., first substrate, temporary auxiliary substrate, and final substrate are required.

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Sakaguchi, et al. provide a process that includes the steps of: forming a nonporous monocrystalline semiconductor layer on a first substrate which includes a porous layer at the surface thereof; bonding a second substrate to the nonporous monocrystalline layer; separating the bonded substrate such that a portion of the porous layer remains on the second substrate and a portion of the porous layer is not removed from the first substrate; removing the portion of the porous layer on the second substrate; and removing the portion of the porous layer remaining on the first substrate. Applicants observe that in the prior art process of Sakaguchi, et al., including each of the five embodiments disclosed therein, one bonding and one detaching step are employed in making the final bonded structure. This is different from the claimed invention wherein two separate bonding and detaching steps are employed. Particularly, Sakaguchi, et al. do not teach or suggest a process which includes the steps *of bonding the upper surface of the semiconductor layer that contains semiconductor devices and is bonded to a first substrate to a temporary auxiliary substrate; detaching the semiconductor layer from said first substrate by breaking apart the porous layer;* ***bonding*** *the bottom surface of the semiconductor layer to a final substrate; and* ***detaching*** *the semiconductor layer from the temporary auxiliary substrate.*

Zavracky, et al. do not alleviate the above defects in Sakaguchi, et al. since the applied secondary reference also does not teach or suggest applicants' claimed method which is recited in Claim 1. Specifically, the applied reference does not teach or suggest a method that includes the steps of bonding the upper surface of the semiconductor layer that contains semiconductor devices and is bonded to a first substrate to a temporary auxiliary substrate; detaching the semiconductor layer from said

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first substrate by breaking apart the porous layer; bonding the bottom surface of the semiconductor layer to a final substrate; and detaching the semiconductor layer from the temporary auxiliary substrate.

Zavracky, et al. provide a method of forming a panel display using thin films of essentially single crystal silicon in which transistors are fabricated to control each pixel of the display. In accordance with a preferred embodiment of Zavracky, et al., a thin essentially single crystal Si film is formed on a release substrate. Transistors and pixel electrodes are formed on the thin essentially single crystal Si film and then the porous release substrate is removed from the structure by etching. A final substrate may then be formed over the entire structure providing the structure shown, for example, in FIG. 2L. Thus, in accordance with the disclosure of Zavracky, et al., two substrates as well as a single detach and bonding step are required. This is different from the claimed invention which includes the steps of *bonding the upper surface of the semiconductor layer that contains semiconductor devices and is bonded to a first substrate to a temporary auxiliary substrate; detaching the semiconductor layer from said first substrate by breaking apart the porous layer; bonding the bottom surface of the semiconductor layer to a final substrate; and detaching the semiconductor layer from the temporary auxiliary substrate.*

In view of the above remarks, applicants submit that Claims 1-13 of the present application are not rendered obvious from the combined disclosures of Sakaguchi, et al. and Zavracky, et al.

With respect to Claims 14-30, applicants submit that the combined disclosures of Sakaguchi, et al. and Zavracky, et al. do not teach or suggest a method in

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which at least one semiconductor device is processed on a semiconductor layer that is formed on a first substrate comprising a base substrate and an at least partially crystalline porous release layer prior to detaching the semiconductor layer by breaking apart the porous release layer.

Sakaguchi, et al. are defective because in the prior art process the semiconductor devices are formed after wafer bonding and detaching. Applicants find no motivation whatsoever in the disclosure of Sakaguchi, et al. to process semiconductor devices onto a semiconductor layer prior to detaching, as presently claimed. In contrast, Sakaguchi, et al. form the semiconductor devices onto the semiconductor layer after bonding and detaching. The prior art approach of Sakaguchi, et al. is discussed at Page 4, line 22-Page 5, line 21 of the specification of the instant application.

Zavracky, et al. are defective for at least the following reason. Specifically, Zavracky, et al. typically require a thermally stable release layer (e.g., SiO_2) and the use of channels or grooves in the device layer to provide a path for the etchant to reach and dissolve the release layer. Hence, the disclosure of Zavracky, et al. teaches and suggests that the channels and grooves are necessary to release the porous layer from the semiconductor layer containing devices thereon. The need for channels and grooves in the Zavracky, et al. process is undesirable since formation of the same may damage the devices present on the device layer. Applicants observe that the combined disclosures of Sakaguchi, et al. and Zavracky would lead to a method in which channels and grooves are required to detach the semiconductor layer containing semiconductor devices from a porous release layer. Thus use of channel and grooves is undesirable since the formation of the same may damage the semiconductor devices.

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In view of the above remarks, the combination of Sakaguchi, et al. and Zavracky, et al. does not render Claims 14-30 obvious. Applicants observe that the above remarks are also applicable to Claims 1-13.

The §103 rejection also fails because there is no motivation in the applied references which suggest modifying the disclosed methods to include the various features of the presented claimed invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d, 1260, 1266, 23 USPQ F2d. 1780, 1783-4 (Fed.Cir. 1992).

The rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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